REMARKS

This application has been reviewed in light of the Office Action dated June 10, 2005.

Claims 17-20 are presented for examination. Claim 17 has been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Claim 17 is the only independent claim. Favorable review is respectfully requested.

Claims 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tokuda et al. (U.S. Pat. No. 5,870,289) in view of Ahn et al. (U.S. Pat. 6,586,835). The applicants respectfully submit that amended independent claim 17 is patentable over the art cited by the Examiner, for the following reasons.

The present invention, as defined in claim 17, is directed to a semiconductor device having a plurality of chips. A support is attached to the chips on the back surfaces thereof; the chips are arranged on the support in a planar horizontal structure with a previously formed filling between the chips (see specification, Fig. 3D). Two additional layers are recited: (1) a first layer disposed on the front surfaces of the chips with a first surface being in contact with the front surfaces of the chips; and (2) a second layer attached to the first layer on the second surface of the first layer.

It is explicitly recited that the first layer is formed of a solid dielectric material (e.g. polyimide, as taught in the specification at page 8, lines 6-9, with reference to Figure 2B). The first layer has vias formed therein, with studs disposed in the vias. The second layer is explicitly recited as being formed of a solid dielectric material and having conducting pads on a surface of the second layer in contact with the first layer (see specification, page 7, line 31, to page 8, line 14, and Figure 2B). Furthermore, the second layer includes electrical wiring connecting to the chips through the studs and the conducting pads. The conducting pads are on a surface in contact with the first layer and are in registration with the vias; each conducting pad forms an end of the corresponding via. It follows that the vias extend through the first layer so that the studs therein contact the conducting pad, but the vias do not extend

into the second layer. These features of the invention are clearly shown in Figures 2B and 3A of the specification.

Tokuda et al. is understood to disclose a chip connection structure having through-hole connections through an adhesive film and a wiring substrate. In Tokuda et al. an adhesive film 30 (see Figure 1; also film 430 in Figure 6) is used to attach a chip to a wiring substrate. This layer is not understood to be equivalent to the solid dielectric layer of the present invention; it more closely resembles the optional adhesive layer 28 shown in Figure 2B of the specification. Accordingly, it is submitted that Tokuda et al. does not suggest a first layer having the features recited in claim 17.

In addition, Tokuda et al. teaches a through-hole connection 40 extending through the wiring substrate, connecting to wiring on a side of the substrate opposite the adhesive film. This is contrary to the present invention, in which each conducting pad (on a surface in contact with the first layer) forms an end of the corresponding via. Assuming *arguendo* that the through-holes of Tokuda et al. are equivalent to the vias of the present invention, it is clear from Figure 3 of Tokuda et al. that those vias extend through the wiring substrate, whether or not wiring is present on the surface of the wiring substrate closest to the chip. One following the teaching of Tokuda et al. in making stud/via connections between a wiring layer and a chip would form vias through the wiring substrate with conducting pads on the surface remote from the chip, instead of forming vias in a first layer with conducting pads at the end of the vias on a surface in contact with that layer (compare Figure 3 of Tokuda et al. with Figure 3A of the specification).

Tokuda et al. thus does not teach or suggest that the first layer is formed of a solid dielectric material, or that a conducting pad forms an end surface of the corresponding via. Accordingly, these features of the present invention would not have been obvious from Tokuda et al.

Ahn is understood to disclose a circuit package in which thermoelectric cooling is provided. Ahn does not disclose or suggest a semiconductor device with the features of the present invention. In particular, Ahn does not suggest a wiring layer in contact with a first layer making stud/via connections to chips, as in the present invention. It therefore is

submitted that Ahn does not remedy the above-noted defects of Tokuda et al. as a reference against the present invention. One might be motivated to combine Ahn with Tokuda et al. to provide cooling for an integrated package having chips and a wiring substrate. Such a combination still would not have the features of the present invention. In particular, a combination of Tokuda et al. and Ahn still would not suggest a second layer with conducting pads as recited in claim 17.

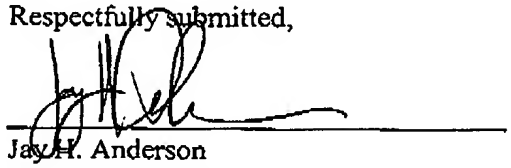
Accordingly, the invention of claim 17 would not have been obvious from either of the cited references, or from a combination thereof.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claims are also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable consideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



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